

2858 #6
ID
7/18/02



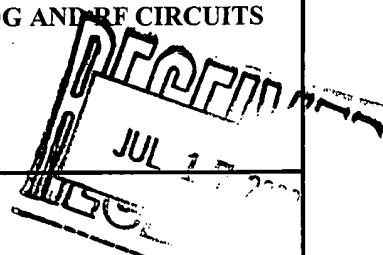
TRANSMITTAL LETTER
(General - Patent Pending)

Docket No.
P 6079.11005

In Re Application of: **Voorakaranam et al.**

Serial No. 09/837,887	Filing Date April 18, 2001	Examiner	Group Art Unit 2858
---------------------------------	--------------------------------------	----------	-------------------------------

Title: **METHOD AND APPARATUS FOR LOW COST SIGNATURE TESTING FOR ANALOG AND RF CIRCUITS**



TO THE COMMISSIONER OF PATENTS AND TRADEMARKS:

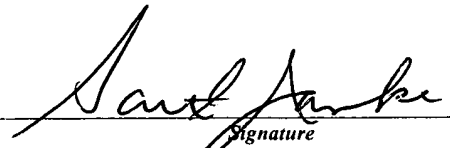
Transmitted herewith is:

Information Disclosure Citation w/references, Certificate of First Class Mail

RECEIVED
JUL 15 2002
Technology Center 2100

in the above identified application.

- ☒ No additional fee is required.
- ☐ A check in the amount of _____ is attached.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **02-2451** as described below. A duplicate copy of this sheet is enclosed.
 - ☐ Charge the amount of _____
 - ☒ Credit any overpayment.
 - ☒ Charge any additional fee required.


Signature

Garth Janke, Reg No. 40,662
Birdwell Janke & Durando, PLC
1100 SW Sixth Avenue, Suite 1400
Portland, Oregon 97204
(503) 228-1841

Dated: **April 18, 2002**

RECEIVED
APR 25 2002
TECHNOLOGY CENTER 2800

I certify that this document and fee is being deposited on **April 18, 2002** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.



Signature of Person Mailing Correspondence

Chris Pellechi

Typed or Printed Name of Person Mailing Correspondence

CC:

CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8)

Applicant(s): Voorakaranapalli et al

Docket No.

P 6079.11005

Serial No.

09/837,887

Filing Date

APR 24 2002

April 18, 2001

Examiner

Group Art Unit

2858

Invention: METHOD AND APPARATUS FOR LOW COST SIGNATURE TESTING FOR ANALOG AND RF CIRCUITS

RECEIVED

JUL 15 2002

Technology Center 2100

I hereby certify that this Information Disclosure Citation w/ references, transmittal ltr
(Identify type of correspondence)

is being deposited with the United States Postal Service as first class mail in an envelope addressed to: The

Assistant Commissioner for Patents, Washington, D.C. 20231 on April 18, 2002
(Date)

Chris Pellechi

(Typed or Printed Name of Person Mailing Correspondence)



(Signature of Person Mailing Correspondence)

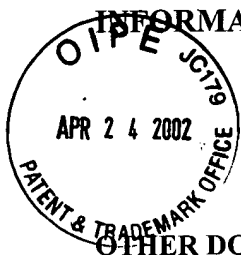
Note: Each paper must have its own certificate of mailing.

RECEIVED

APR 25 2002

TECHNOLOGY CENTER 2800

OIPF INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>							Docket Number (Optional) P 6079:11005	Application Number 09/837,887	
							Applicant(s) Voorakaranam et al.		
							Filing Date April 18, 2001	Group Art Unit 2858	
U.S. PATENT DOCUMENTS									
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE		
		6,114,858	9/5/00	Kasten					
							RECEIVED		
							JUL 15 2002		
							Technology Center 2100		
							TECHNOLOGY CENTER 2800		
							APR 25 2002		
							RECEIVED		
FOREIGN PATENT DOCUMENTS									
	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation		
							YES	NO	
OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>									
		S. J. Tsai, "Test Vector Generation for Linear Analog Devices," International Test Conference (1991) 592-597							
		W. Lindermeir, H.E. Graeb & K.J. Antreich, "Design of Robust Test Criteria in Analog Testing," International Conference on Computer-Aided Design" (1995) 604-611							
EXAMINER					DATE CONSIDERED				
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.									



INFORMATION DISCLOSURE CITATION

Attorney Docket **Serial No.**
P 6079.11005 09/837,887
Voorakaranam et al. et al.
Filing **Group**
April 18, 2001 2858

RECEIVED

JUL 15 2002

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

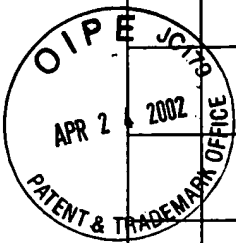
Technology Center 2100

		R. Voorakaranam & A. Chatterjee, "Test Generation for Accurate Prediction of Analog Specifications," IEEE VLSI Test Symposium (2000) 137-142
		J.H. Friedman, "Multivariate Adaptive Regression Splines," The Annals of Statistics, Vol. 19, No. 1, 1-141
		P.A. Variyam and A. Chatterjee, "Specification-Driven Test Design for Analog Circuits," International Symposium on Defect and Fault Tolerance in VLSI Systems (1998) 335-340
		T. Wilson, "Test Challenges for Next-Generation RF Devices," EE Evaluation Engineering, Vol. 39, No. 11 (2000) 31-37
		D.A. Coley, An Introduction to Genetic Algorithms for Scientists and Engineers, World Scientific (1996) 1-16
		Cadence SpectreRF Simulator User Guide (December 1999)
		Cadence OCEAN Reference Guide (December 1999)
		RF Micro-Devices, Low Noise Amplifier/Mixer (March 2001)
		S. Cherubal & A. Chatterjee, "Parametric Fault Diagnosis for Analog Systems Using Functional Mapping," Proceedings, Design, Automation and Test in Europe (1999) 195-200
		P.N. Variyam & A. Chatterjee, "Enhancing Test Effectiveness for Analog Circuits Using Synthesized Measurements," VLSI Test Symposium (1998) 132-137
		A. Walker, W. Alexander & P.K. Lala, "Fault Diagnosis in Analog Circuits Using Element Modulation," IEEE Design and Test of Computers (March 1992) 19-29
		H. Walker & S.W. Director, "VLASIC: A Catastrophic Fault Yield Simulator for Integrated Circuits," IEEE Transactions on Computer-Aided Design (October 1986) 541-556
		N.Nagi, A. Chatterjee, A. Balivada & J.A. Abraham, "Fault-Based Automatic Test Generation for Linear Analogy Devices," Proceedings, International Conference on Computer-Aided Design (1993) 88-91
		M. Salamani & B. Kaminska, "Multifrequency Analysis of Faults in Analog Circuits," IEEE Design and Test of Computers (1995) 70-80
		B. Hamida, K. Saab, D. Marche, B. Kaminska & G. Qusnel, "LIMSoft: Automated Tool for Design and Test Integration of Analog Circuits," International Test Conference (1996) 571-580
		H.H. Zheng, A. Balivada & J.A. Abraham, "A Novel Test Generation Approach for Parametric Faults in Linear Analog Circuits," VLSI Test Symposium (1996) 470-475

Examiner

Date Considered

RECEIVED
APR 25 2002
TECHNOLOGY CENTER 2800



RECEIVED

JUL 15 2002

Technology Center 2100

		A. Balivada, J. Chen & J.A. Abraham, "A Novel Test Generation Approach for Parametric Faults in Linear Analog Circuits," VLSI Test Symposium (1996) 470-475
		A. Abderrahman, E. Cerny & B. Kaminska, "CLP-Based Multifrequency Test Generation for Analog Circuits," VLSI Test Symposium (1997) 158-165
		G. Devarayanadurg & M. Soma, "Dynamic Test Signal Design for Analog ICs," Proceedings, International Conference on Computer-Aided Design (1995) 627-629
		W. Verhaegen, G. Van de Plas & G. Gielen, "Automated Test Pattern Generation for Analog ICs," Proceedings, VLSI Test Symposium (1997) 296-301
		J.B. Brockman & S.W. Director, "Predictive Subset Testing: Optimizing IC Parametric Performance Testing for Quality, Cost and Yield," IEEE Transactions on Semiconductor Manufacturing, Vol. 2 (1989) 104-113
		W. Maly & Z. Pizlo, "Tolerance Assignment for IC Selection Tests," IEEE Transactions on Computer-Aided Design (April 1985) 156-162
		T.M. Souders & G.N. Stenbakken, "Cutting the High Cost of Testing," IEEE Spectrum (March 1991) 48-51
		S.D. Huss & R.S. Gyurcsik, "Optimal Ordering of Analog IC Tests to Minimize Time," Proceedings, Design Automation Conference (1991) 494-499
		L. Milor & A.L. Sangiovanni-Vincentelli, "Minimizing Production Test Time to Detect Faults in Analog Circuits," IEEE Transactions on Computer-Aided Design, Vol. 13 (1994) 796-813
		M.J. Marlett & J.A. Abraham, "DC-IATP: An Iterative Analog Circuit Test Generation Program for Generating DC Single Pattern Tests," Proceedings, IEEE International Test Conference (1988) 839-845
		G. Devarayanadurg & M. Soma, "Analytic Fault Modeling and Static Test Generation for Analog ICs," International Conference for Computer-Aided Design (1994) 44-47
		W.M. Lindermeir, H.E. Graeb & K.J. Antreich, "Design Based Analog Testing by Characteristic Observation Inference," International Conference for Computer-Aided Design (1995) 620-626
		C.Y. Pan & K.T. Cheng, "Implicit Functional Testing for Analog Circuits," VLSI Test Symposium (1996) 489-494
		P.N. Variyam & A. Chatterjee, "Test Generation for Comprehensive Testing of Linear Analog Circuits Using Transient Response Sampling," International Conference on Computer-Aided Design (1997) 382-385
		K.J. Antreich, H.E. Graeb & C.U. Wieser, "Circuit Analysis and Optimization Driven by Worst Case Distances," IEEE Transaction on CAD, Vol. 13 (1994) 57-71
		D.G. Saab, Y.G. Saab & J.A. Abraham, "CRIS: A Test Cultivation Program for Sequential VLSI Circuits," Proceedings: International Conference on Computer-Aided Design (1992) 216-219
		G. Devarayanadurg, P. Goteti & M. Soma, "Hierarchy Based Statistical Fault Simulation of Mixed-Signal ICs," International Test Conference (1996) 521-527
		A. Basilevsky, "Statistical Factor Analysis and Related Methods, Theory and Applications," Wiley Series in Probability and Mathematics (1994)

Examiner

Date Considered

RECEIVED
APR 25 2002
TECHNOLOGY CENTER 2800



		I.T. Joliffe, "Discarding Variables in a Principle Component Analysis, I. Artificial Data," Applied Statistics, Vol. 22 (1973) 21-31
		L. Milor & A.L. Sangiovanni-Vincentelli, "Optimal Test Set Design for Analog Circuits," International Conference on Computer-Aided Design (1990) 294-297
		A.V. Gomes & A. Chatterjee, "Minimal Length Diagnostic Tests for Analog Circuits Using Test History," Design, Automation and Test in Europe (1999) 189-194
		MATLAB Optimization Toolbox User's Guide

RECEIVED

Examiner	Date Considered	JUL 15 2002 Technology Center 2100
----------	-----------------	---------------------------------------

Page 4 of 4

RECEIVED
APR 25 2002
TECHNOLOGY CENTER 2800